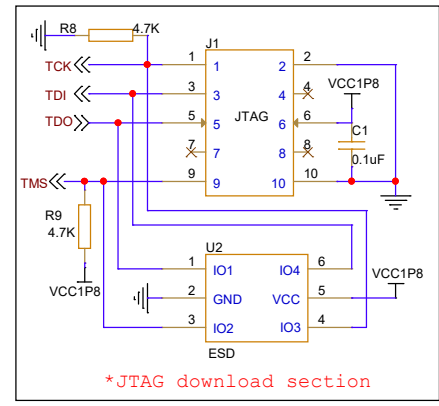
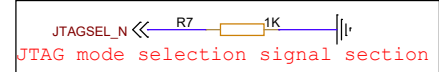
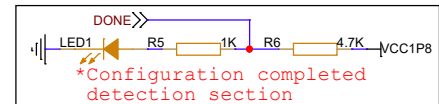
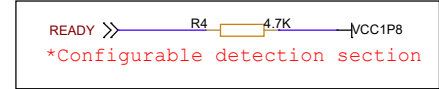
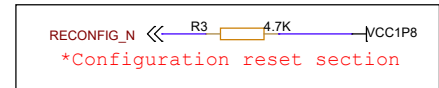
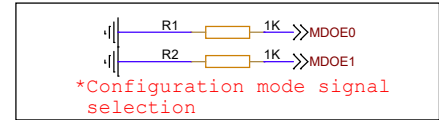
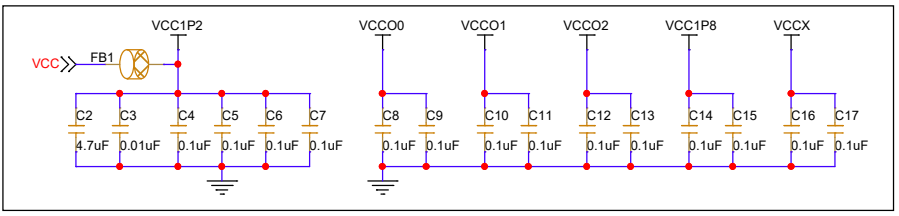
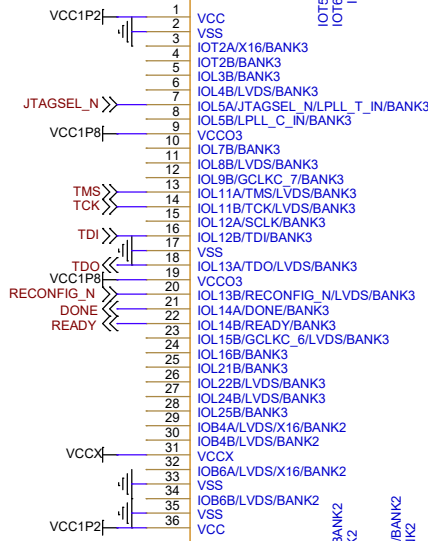
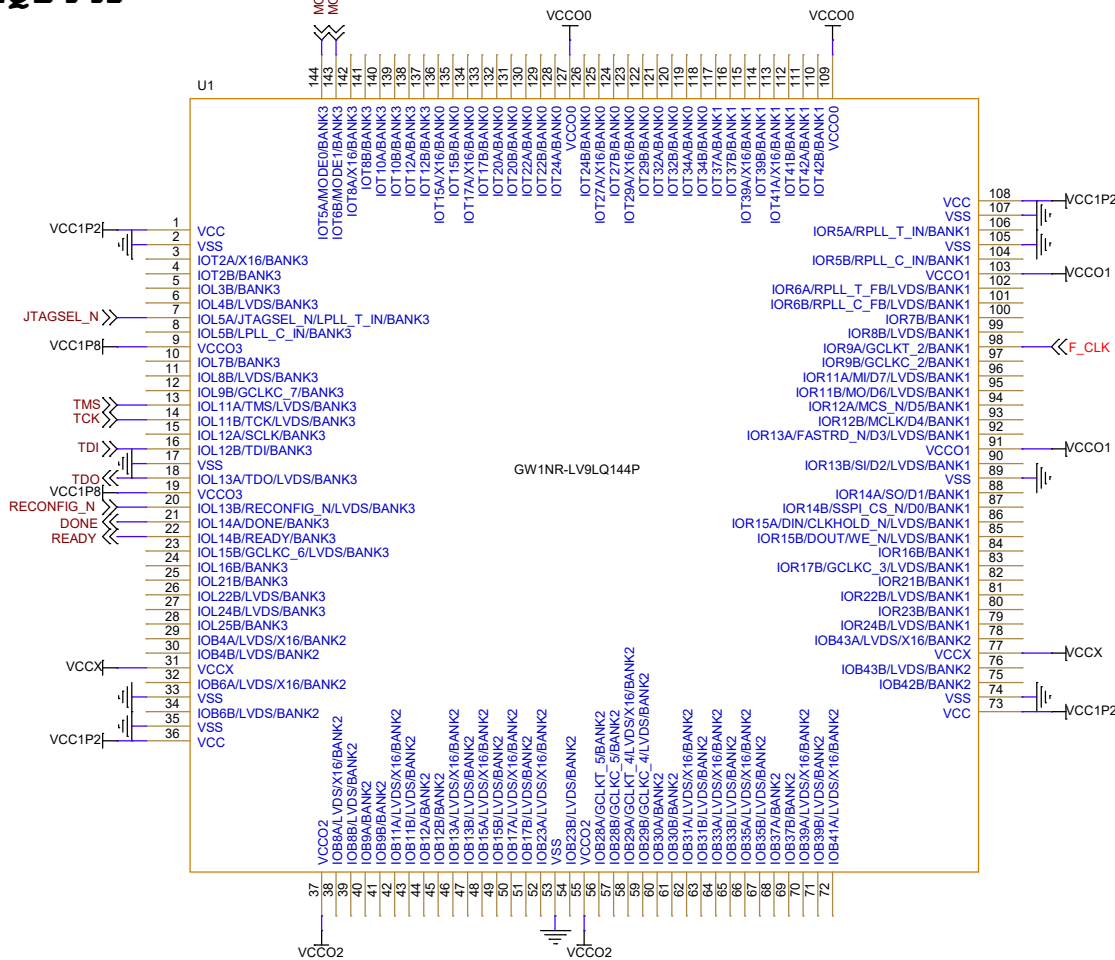
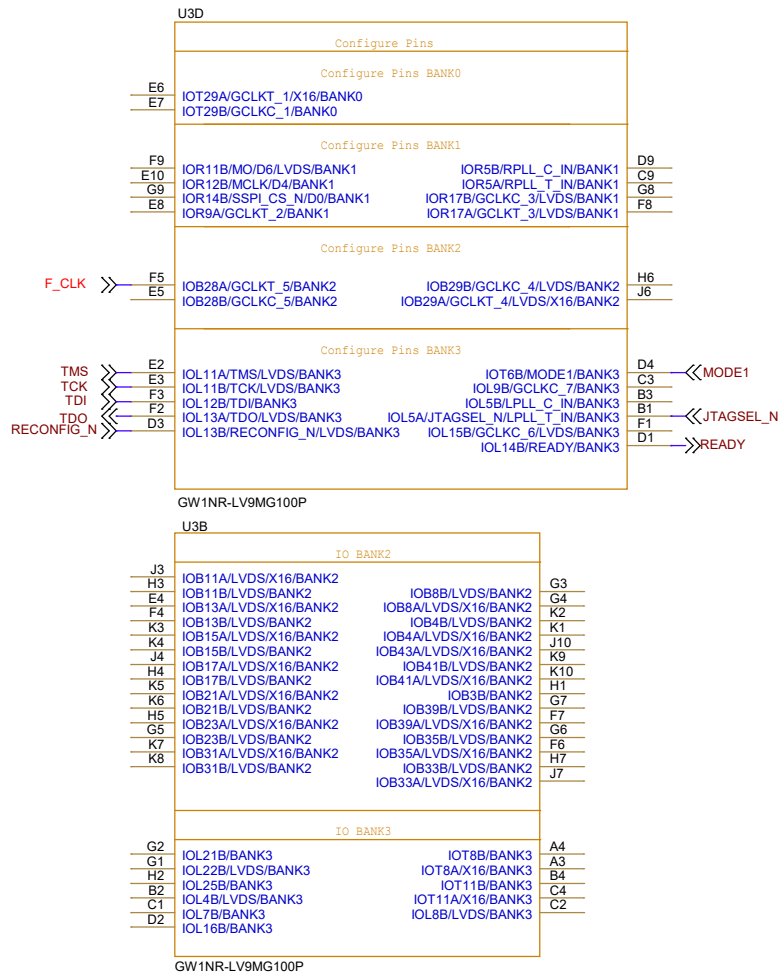




Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

|                              |                        |               |
|------------------------------|------------------------|---------------|
| Title                        |                        |               |
| GOWIN Minimum System Diagram |                        |               |
| Size                         | Document Number        | Rev           |
| B                            | GW1NR-LV9LQ144P        | 2.3           |
| Date:                        | Friday, March 07, 2025 | Sheet 1 of 12 |

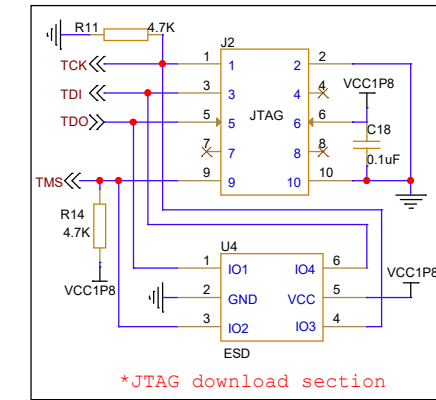
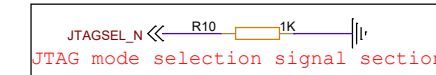
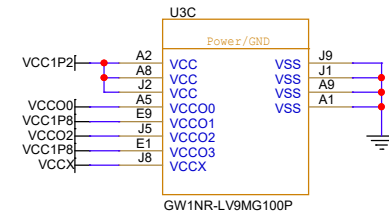
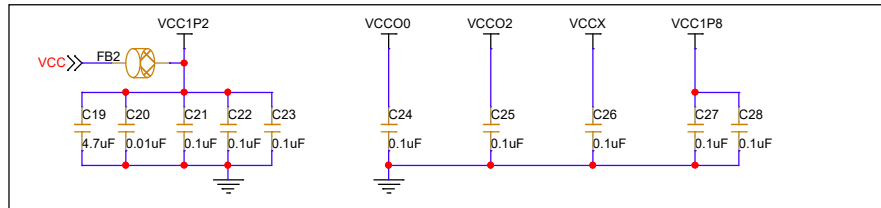
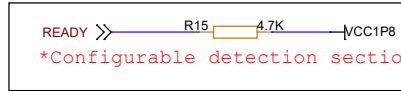
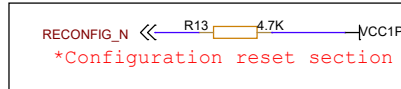
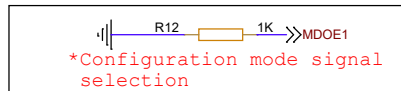
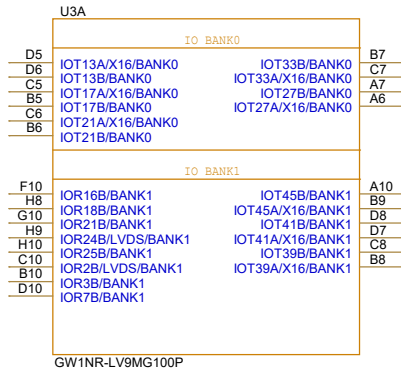


Notes:

1.F\_CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

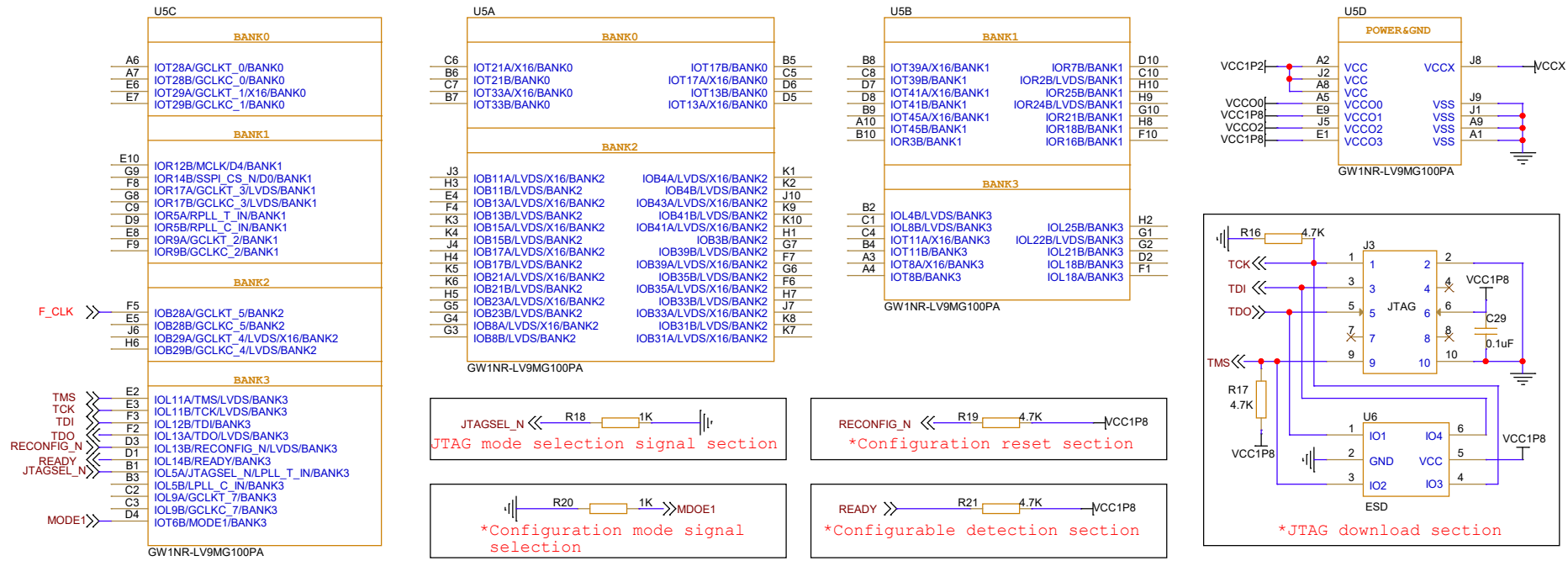
2.It is recommended that add an ESD protection chip to the JTAG download circuit.



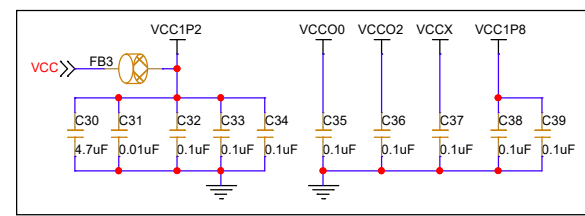
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| Title                        |                                 |         |
| GOWIN Minimum System Diagram |                                 |         |
| Size B                       | Document Number GW1NR-LV9MG100P | Rev 2.3 |
| Date: Friday, March 07, 2025 | Sheet 2 of 12                   |         |

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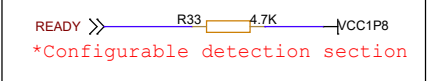
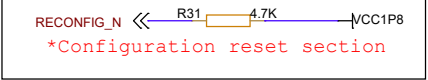
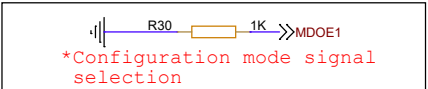
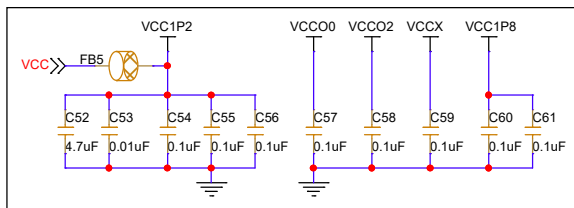
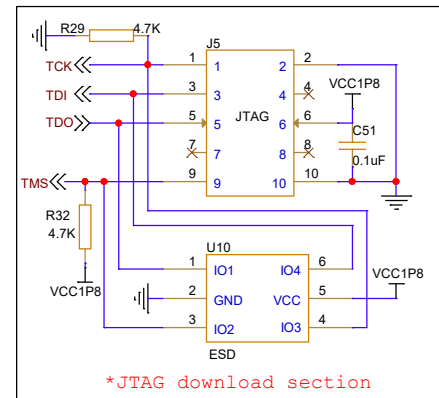
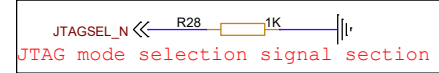
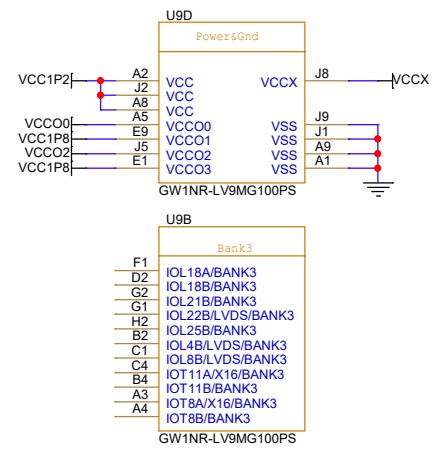
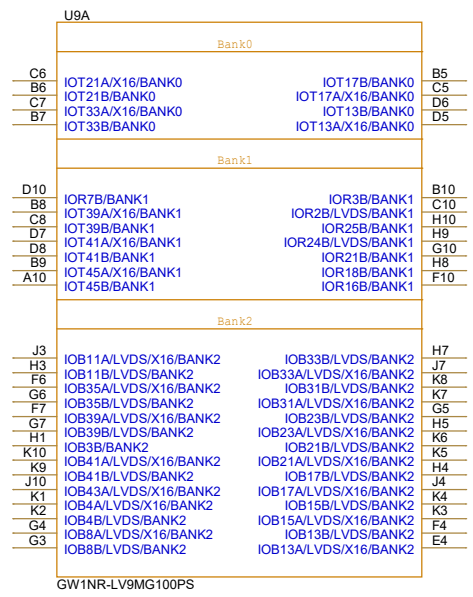
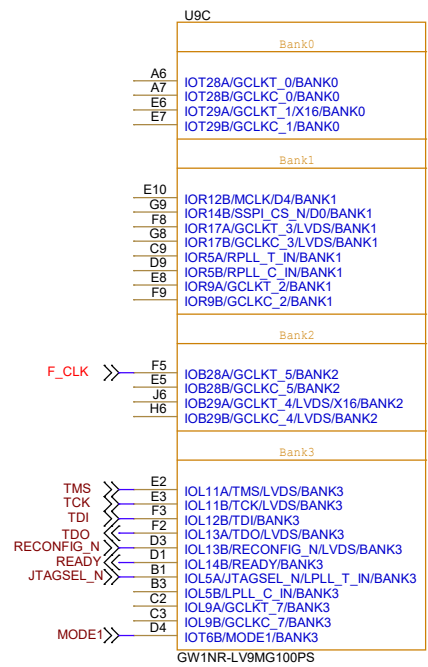
D



Notes:  
1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.



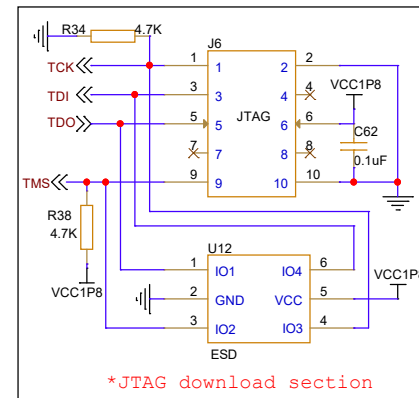
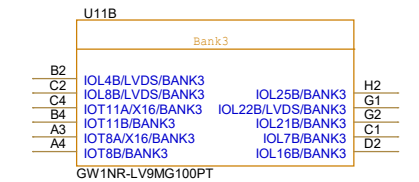
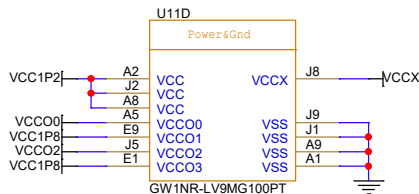
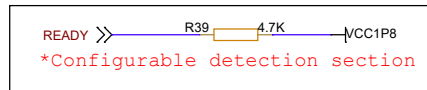
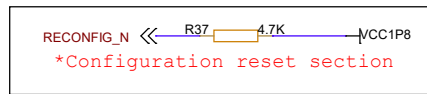
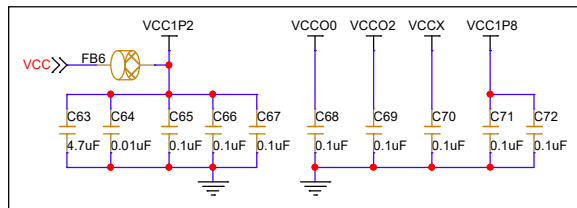
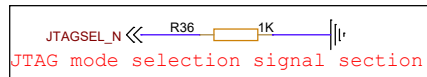
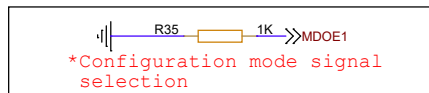
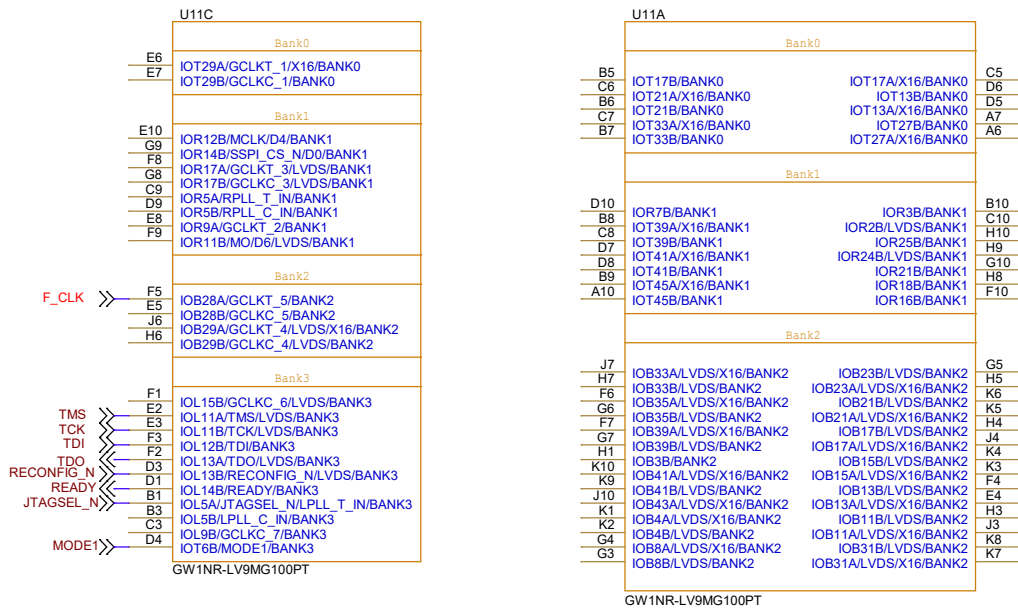




Notes:

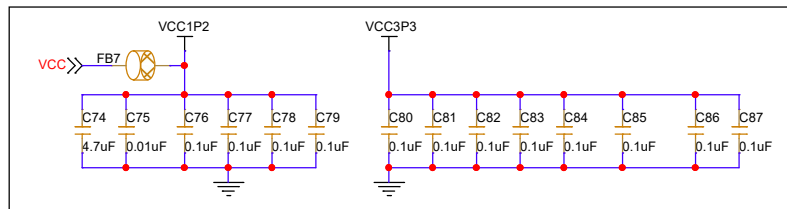
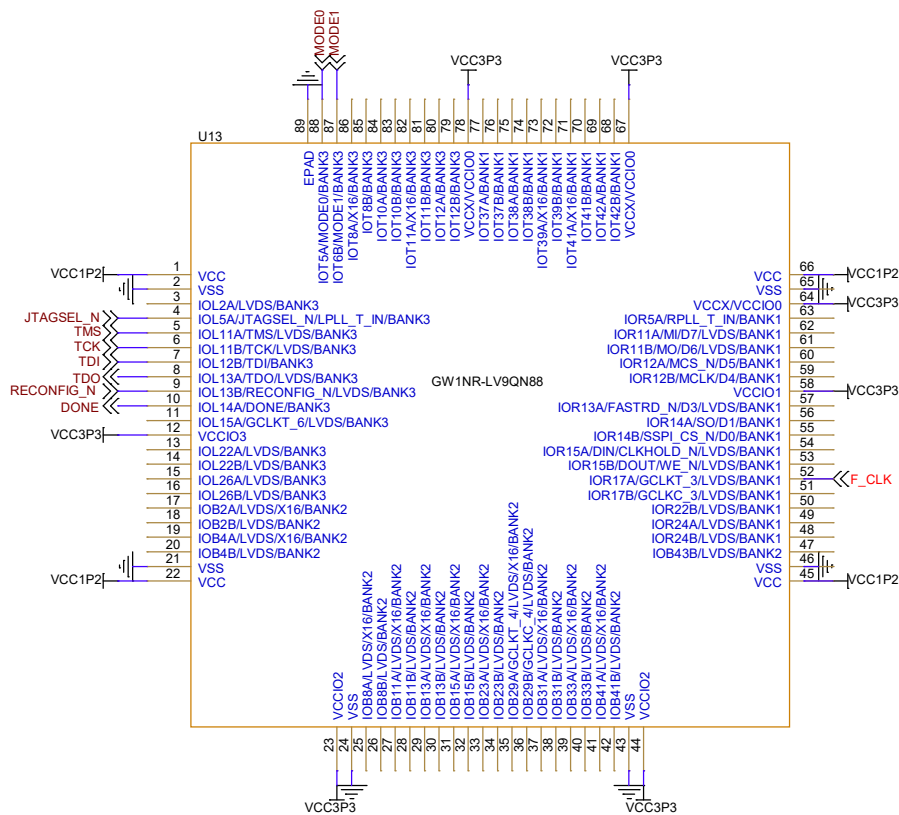
1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.



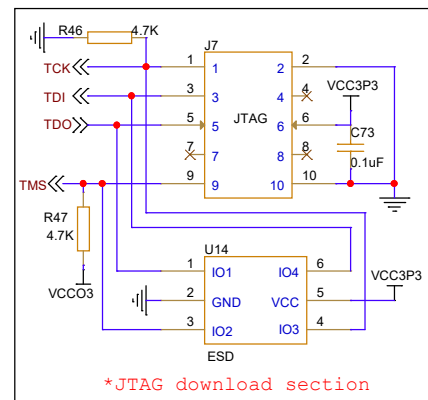
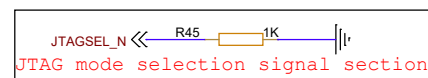
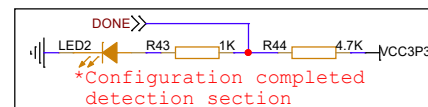
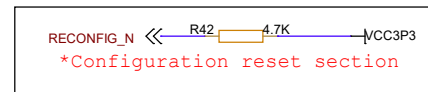
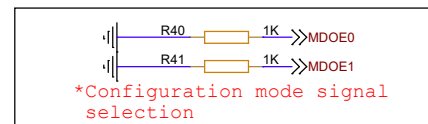
Notes:

- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

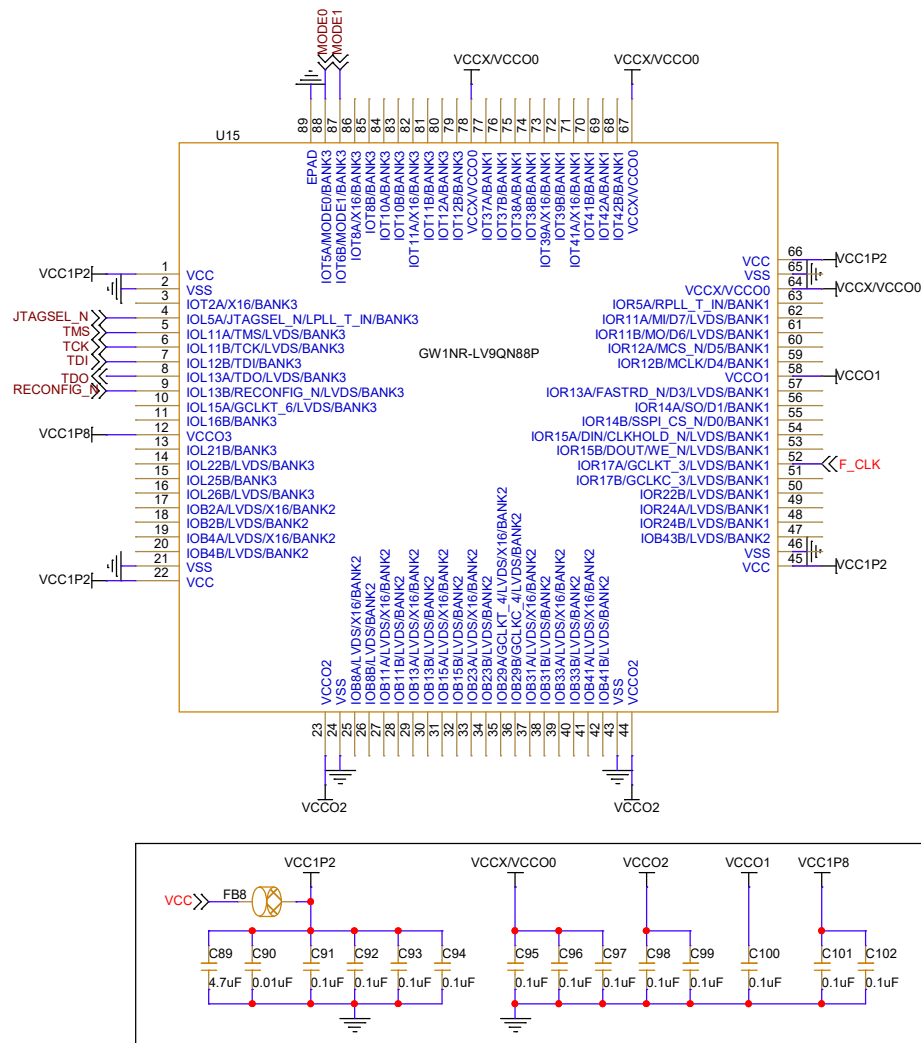


Notes:

- 1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

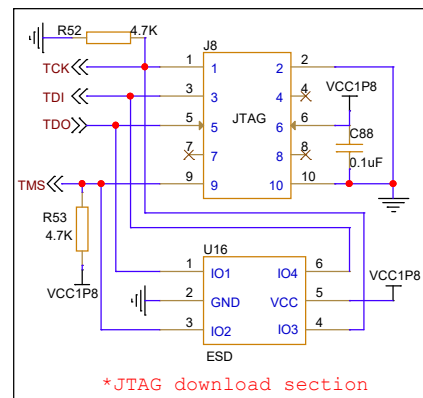
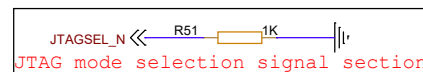
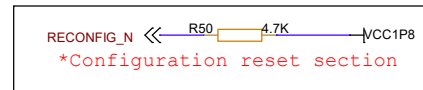
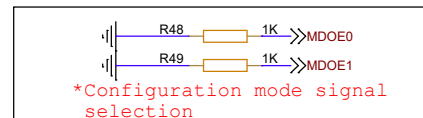


|                              |                        |               |
|------------------------------|------------------------|---------------|
| Title                        |                        |               |
| GOWIN Minimum System Diagram |                        |               |
| Size                         | Document Number        | Rev           |
| B                            | GW1NR-LV9QN88          | 2.3           |
| Date:                        | Friday, March 07, 2025 | Sheet 7 of 12 |

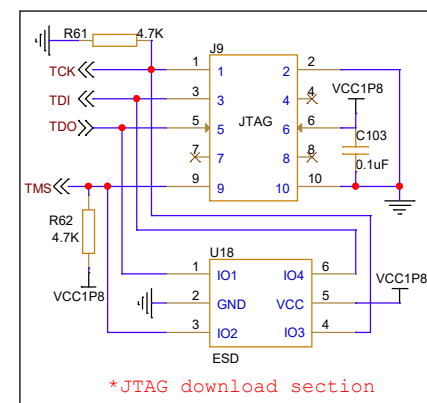
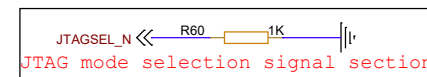
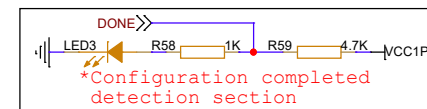
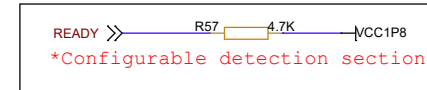
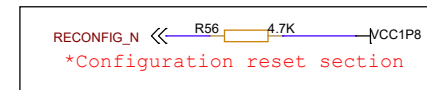
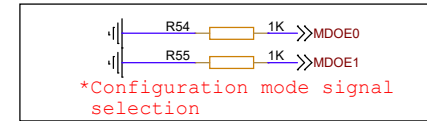
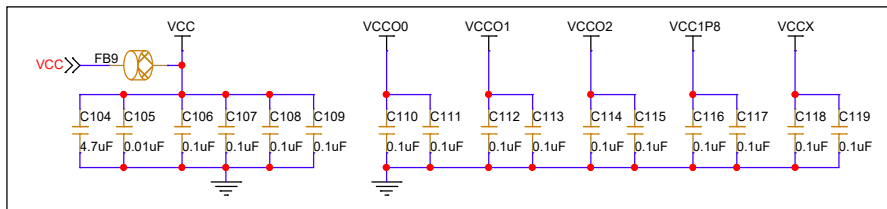
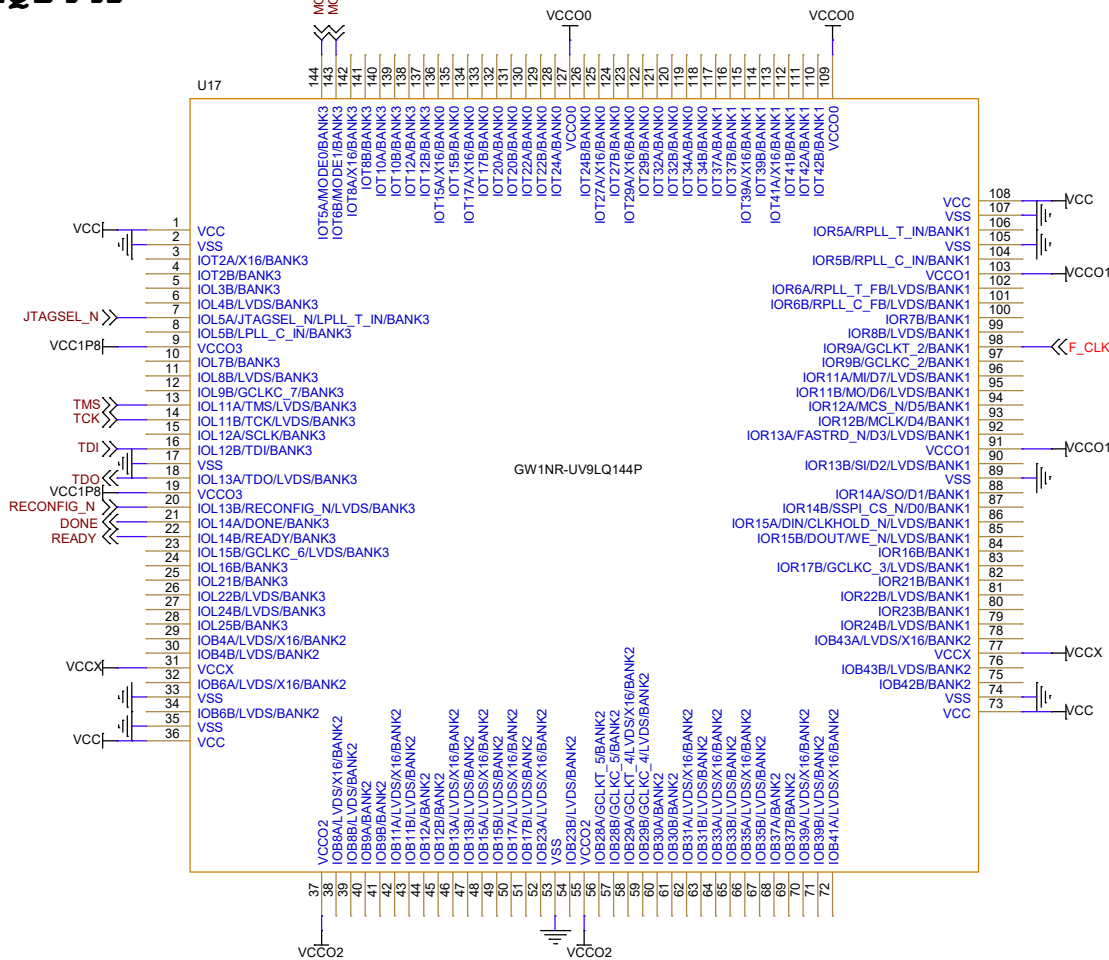


1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

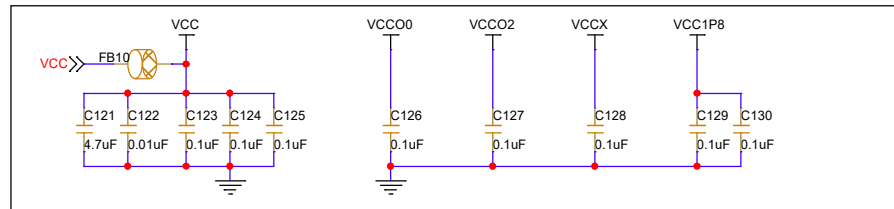
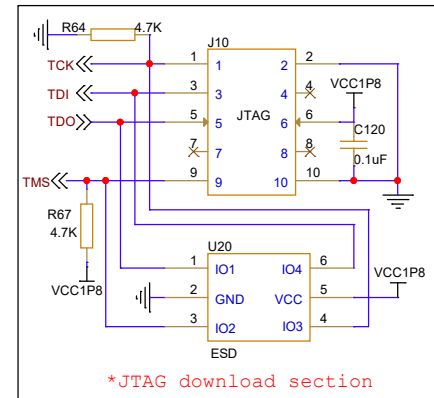
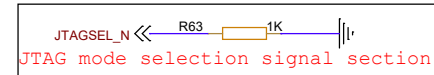
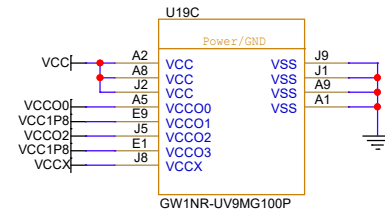
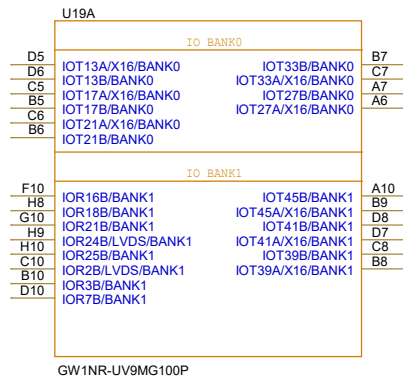


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|                              |                                   |               |        |
| Title                        |                                   |               |        |
| GOWIN Minimum System Diagram |                                   |               |        |
| Size B                       | Document Number<br>GW1NR-LV9QN88P |               | Rev 2. |
| Date:                        | Friday, March 07, 2025            | Sheet 8 of 12 |        |



Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

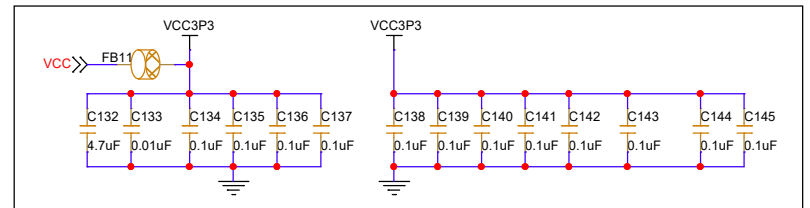
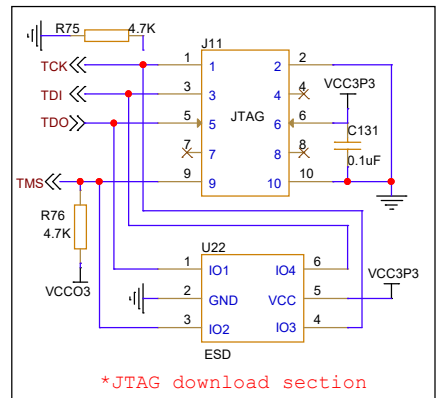
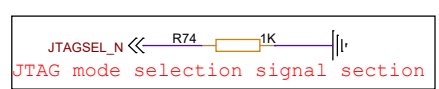
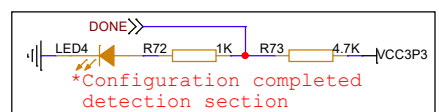
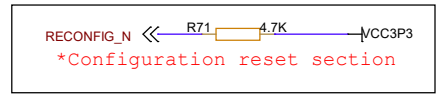
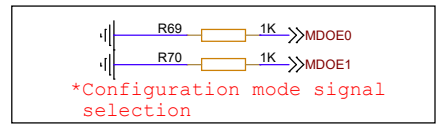
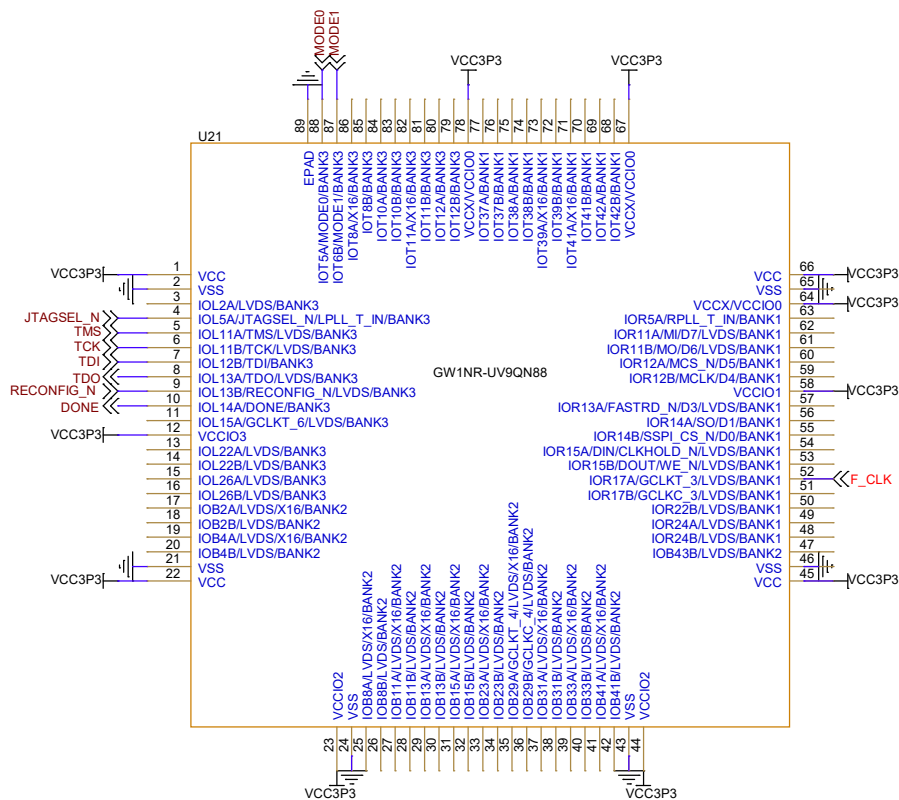
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| GOWIN Minimum System Diagram |                        |               |
| Size                         | Document Number        | Rev           |
| B                            | GW1NR-UV9LQ144P        | 2.3           |
| Date:                        | Friday, March 07, 2025 | Sheet 9 of 12 |



Notes:

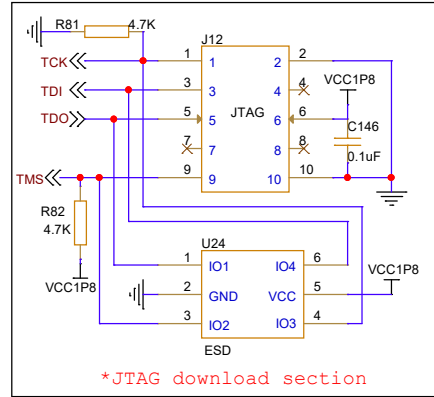
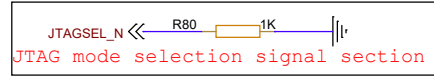
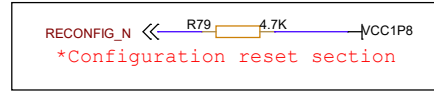
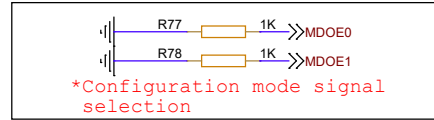
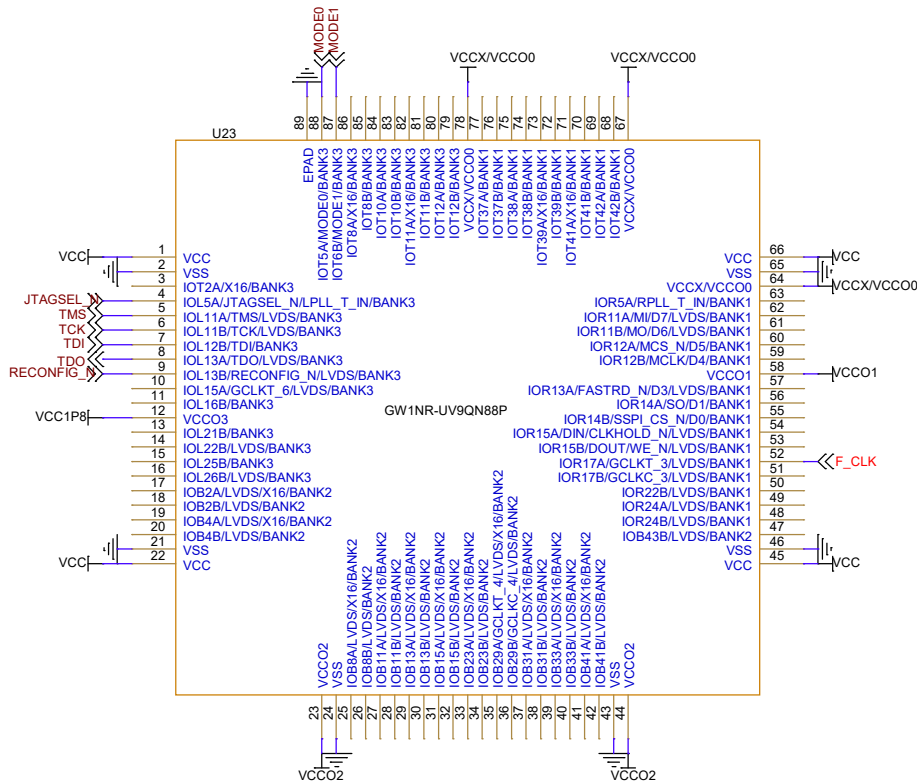
- 1.F\_CLK signal is an external input clock signal.  
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

|                              |                        |                |
|------------------------------|------------------------|----------------|
| Title                        |                        |                |
| GOWIN Minimum System Diagram |                        |                |
| Size                         | Document Number        | Rev            |
| B                            | GW1NR-UV9MG100P        | 2.3            |
| Date:                        | Friday, March 07, 2025 | Sheet 10 of 12 |



Notes:  
1.F CLK signal is an external input clock signal.  
It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

|                              |                        |       |          |
|------------------------------|------------------------|-------|----------|
| Title                        |                        |       |          |
| GOWIN Minimum System Diagram |                        |       |          |
| Size                         | Document Number        | Rev   |          |
| B                            | GW1NR-UV9QN88          | 2.3   |          |
| Date:                        | Friday, March 07, 2025 | Sheet | 11 of 12 |



Notes:  
 1.F CLK signal is an external input clock signal.  
 It is recommended that F\_CLK signal be provided through an active oscillator crystal.  
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

|                              |                        |                |
|------------------------------|------------------------|----------------|
| Title                        |                        |                |
| GOWIN Minimum System Diagram |                        |                |
| Size                         | Document Number        | Rev            |
| B                            | GW1NR-UV9QN88P         | 2.3            |
| Date:                        | Friday, March 07, 2025 | Sheet 12 of 12 |